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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/676,844	09/29/2000	Bryan R White	10559-165001/P8249	3643

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EXAMINER	
MONESTIME, MACKLY	

ART UNIT	PAPER NUMBER
2676	20

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/676,844	Applicant(s) WHITE, BRYAN R	
	Examiner Mackly Monestime	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The amendment received on April 15, 2004 has entered and carefully considered. Claims 1-16 are still pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 7-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nielsen et al (US Patent No. 6,104,417) in view of Lohman (US Patent No. 6,714,957).

4. Nielsen et al were cited in the last office action.

5. As per claims 1 and 13, Nielsen et al substantially disclosed the invention as claimed, including a memory controller hub comprising: an internal graphics subsystem adapted to perform graphics operations on data (Fig. 2B; Item No. 218); determining whether the memory controller hub is operably coupled to an external graphics controller or performs graphics operations on data using internal graphics subsystem (Fig. 2B, Items No. 218, 210, 212).

Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and

adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data. However, Nielsen et al did disclose a rendering engine that supports a frame buffer address translation buffer (TLB) to translate frame buffer (x,y) addresses into physical memory addresses, wherein the TLB is loaded by CPU with the base physical memory addresses (Fig. 2B, Items No 208, 206). Moreover, the concepts and associated advantages of using a cache to store addresses of location physical memory; thus, as is well known in the art, both caches and buffers are often used in a similar manner (i.e. quick access to store data). Furthermore, Lohman disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data (Fig. 2, Item No. 120; col. 6, lines 18-25). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the cache disclosed by Lohman into the system of Nielsen et al because doing so would provide a cache which can be share by a memory controller as well a graphics controller in the computer system without transferring data between multiple dedicated memory units; thereby enhance the flexibility of the computer system.

6. As per claim 7, Nielsen et al substantially disclosed the invention as claimed, including a CPU (Fig. 2, Item No. 206); a display device (col. 2, lines 48-50); a system memory adapted to store video data and non-video data (Fig. 2, Item No. 202); and a memory controller hub coupled to the CPU (Fig. 2, Item No. 204) and coupled to the

system memory (Fig. 2, Item No. 202), the memory controller hub comprising: an internal graphics subsystem adapted to perform graphics operations on data (Fig. 2B; Item No. 218).

Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data. However, Nielsen et al did disclose a rendering engine that supports a frame buffer address translation buffer (TLB) to translate frame buffer (x,y) addresses into physical memory addresses, wherein the TLB is loaded by CPU with the base physical memory addresses (Fig. 2B, Items No 208, 206). Moreover, the concepts and associated advantages of using a cache to store addresses of location physical memory; thus, as is well known in the art, both caches and buffers are often used in a similar manner (i.e. quick access to store data). Furthermore, Lohman disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data (Fig. 2, Item No. 120; col. 6, lines 18-25). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the cache disclosed by Lohman into the system of Nielsen et al because doing so would provide a cache which can be share by a memory controller as well a graphics controller in the computer system without transferring data

between multiple dedicated memory units; thereby reducing the overall amount of traffic passing between memory bridge and system memory.

7. As per claims 2-3 and 8-9, Nielsen et al disclosed a dedicated bus interface coupling to the graphics controller to the memory controller hub (col. 4, lines 19-21).

8. Claims 4-6, 10-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nielsen al in view of Lohman as applied to claims 1-3, 7-9 and 13 above, and further in view of Hussain et al (US Patent No. 6,667,745).

9. Hussain et al were cited in the last office action.

As per claims 4-6, 10-12 and 14-16, Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data. However, Nielsen et al did disclose a rendering engine that supports a frame buffer address translation buffer (TLB) to translate frame buffer (x,y) addresses into physical memory addresses, wherein the TLB is loaded by CPU with the base physical memory addresses (Fig. 2B, Items No 208, 206). Moreover, the concepts and associated advantages of using a cache to store addresses of location physical memory; thus, as is well known in the art, both caches and buffers are often used in a similar manner (i.e. quick access to store data). Furthermore, Lohman disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data (Fig. 2, Item No.

120; col. 6, lines 18-25). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the cache disclosed by Lohman into the system of Nielsen et al because doing so would provide a cache which can be share by a memory controller as well a graphics controller in the computer system without transferring data between multiple dedicated memory units; thereby reducing the overall amount of traffic passing between memory bridge and system memory.

Nielsen et al did not explicitly disclose that the memory controller is configured to provide a block of linear, virtual memory address for use by graphics subsystem or graphics controller, but did disclose translation hardware that maps virtual addresses of pixel buffers to physical memory locations in unified system memory (col. 6, lines 25-33). However, Hussain disclosed a graphics controller that utilizes tile frame buffer linear mapping system to perform mapping functions that facilitate mapping of linear virtual addresses to a physical memory address (col. 9, lines 25-38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would not only allow the graphics system to communicate information to and from a memory in an efficient manner, including translation or conversion between different virtual address configurations and physical memory address, thereby enhance the processing speed of the graphics system.

Response to Arguments

10. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, Va, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackly Monestime

Patent Examiner

June 1, 2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600